Remarks

Claims 1-24 remain in this application. Claims 1, 11 and 22 have been amended. Claims 1, 11, 17 and 22 are independent claims.

In an Office action dated June 18, 2004, claims 1-4, 9-16 and 22-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. Additionally, claims 4-8 and 17-21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. in view of Quach. In response, independent claims 1, 11 and 22 have been amended to more clearly distinguish the claimed invention from the cited prior art.

It is respectfully asserted that the prior art references, whether taken alone or in combination, do not teach or suggest a volatile memory checker enabled to execute between periods of activity of a device in order to detect soft errors occurring during extended periods of inactivity of the device (claim 1). Nor does the combination of prior art patents teach or suggest that a method of assessing integrity of executable code by performing time-based volatile memory checking routines in response to detecting that the device is in an inactive state, so as to detect soft errors within the executable code, wherein the soft errors are those errors occurring during the inactive state between executions of the executable code (claim 11). Similarly, Jiang et al. and Quach do not render the integrated circuit of claim 17 or the system of claim 22 obvious, since they refer to time-based test initialization for periodic testing (claim 17) and an automated memory checker enabled to execute between periods of activity on a timed basis to detect soft errors occurring during extended periods of inactivity (claim 22).

Reconsideration of the claims in view of the amendments and the remarks that follow is requested.

A. Patentability of Independent Claims 1, 11 and 22

Amended independent claims 1, 11 and 22 each describe error detection between periods of activity. Additionally, each of the three amended independent claims describes the soft errors as being those errors that occur during extended periods of inactivity. Support for the amendments to the independent claims regarding the occurrence of "soft errors" may be found in Paragraph [0004] of the application as originally filed, wherein it is stated that if the executable code is stored in volatile memory during periods of inactivity,

soft errors in the executable code will accumulate and be undetected until the next use.

Regarding independent claim 1, Applicants respectfully submit that the prior art does not teach or suggest memory checking between periods of activity in order to detect soft errors occurring during extended periods of inactivity. The cited reference to Jiang et al. teaches a system and method for detecting process-related failures or "hard failures." Thus, Jiang et al. is concerned with "hard(ware)" errors and its teachings do not refer to detecting "soft(ware)" errors. This is first introduced in column 1, lines 15-42 of the patent, which discusses each category of process-related failure and the manner in which the failures occur. The patent states that DRAM arrays are susceptible to process-related failures, such as those resulting from dust particles on the chips or masks, scratches, and gate oxide pinholes, which may result in shorts or "opens" in the circuit. The classifications of DRAM faults are "stuck-at" faults, "stuck-open" faults, transitions faults, state coupled faults, multiple access faults, and data retention faults. In describing each one of these classes, a single memory cell is referenced. For example, a memory cell is said to be stuck-at if a read from the cell is always at a certain logic value regardless of the action on the cell. A memory cell is said to be stuck-open if it can never be accessed. A memory cell with a data retention fault is one that is unable to retain the charge stored for a minimum required period. In a data retention test, it is determined whether a particular memory cell can retain a value for an entire refresh period (Jiang et al.: column 3, lines 23-36). If a memory cell is unable to retain a value for the refresh period, the address of the failed memory location is written to a test address register. The remainder of the Jiang et al. patent is consistent in its teachings that memory cells with these physical errors are being detected and recorded.

A first fundamental difference between Jiang et al. and the system described in amended claim 1 is that the Jiang et al. patent is concerned with physical defects and not the "soft errors" that occur during extended periods of inactivity of a device between periods of activity of the device. While the "test unit" of Jiang et al. may be implemented in either hardware or software (as noted in the Abstract), the patent is not concerned with soft errors of the type described in the amended claims. Rather, the patent is concerned with process-related failures, such as those resulting from dust particles on the chips or the masks, scratches, and gate oxide pinholes. A second fundamental difference that patentably distinguishes the claimed invention from the teachings of Jiang et al. is that the volatile memory checker

is enabled to execute between periods of activity of the device. In comparison, the testing described in Jiang et al. is intended to identify addresses of memory cells which are incapable of operating as designed, because they are unable to retain data (data retention faults) or have some other fault that prevents proper operation.

The secondary reference to Quach is related to soft errors, but there is no suggestion in either the primary reference to Jiang et al. nor the secondary reference to Quach to modify the system of Jiang et al. to more closely approach Applicants' invention, as now claimed. That is, the two references do not present a *prima facie* case of obviousness with regard to the claims, as amended. Equally importantly, even if one were to modify Jiang et al. to include teachings of Quach, the modification would not render the claimed invention unpatentable under Section 103(a), since neither patent teaches or suggests executing the volatile memory checker between periods of activity. As previously noted, Jiang et al. teaches identifying addresses of cell locations having process-related failures. Since process-related failures result from dust particles on the chips and masks, scratches, and pinholes, the failures are detectable immediately following fabrication processing. There is no motivation to execute volatile memory checking between periods of activity of a device (e.g., a printer) that includes extended periods of inactivity between such periods of activity.

In Quach, the checking occurs while the processor is in its redundant execution mode. This is defined in column 1, lines 61-64 as a condition of detecting errors by processing instructions on duplicate execution cores and comparing results. When an error is detected, the routine switches the processor to its split execution mode, in which each execution core saves uncorrupted data in an associated storage structure to a designated memory location. The routine recovers processor state data from the saved data. As noted in the last sentence in the Abstract of Quach, the error recovery routine returns the processor to the redundant execution mode, initializes each execution core with the recovered processor state data, and returns control of the processor to the program thread that was executing when the soft error was detected. If one were to modify Jiang et al. to include the switching between the modes and the return to execution of the program thread as described in Quach, the system would not include memory checking during periods described in claim 1. Instead, data checking would occur during periods of activity. Therefore, Applicants respectfully submit that amended claim 1 and its dependent claims are in an allowable condition.

Many of the remarks made with regard to the patentability of claim 1 apply equally to the determination of patentability of independent claims 11 and 22. For all three of the amended independent claims, the description of soft errors has been clarified. This distinguishes the invention from detection of hard errors, as taught by the primary reference to Jiang et al. It is respectfully asserted that without the aid of Applicants' pending application, it would not be obvious to modify the teachings of Jiang et al. to detect soft errors. That is, the combination of Jiang et al. and Quach does not present a *prima facie* case of obviousness with regard to the claims, as amended.

Moreover, claims 11 and 22 state that the memory checking is time based. Claim 11 states that the method comprises performing time-based volatile memory checking routines in response to detecting that the device is in an inactive state and a preselected time period has elapsed. Claim 22 describes the system as comprising an automated memory checker enabled to execute between periods of activity and being configured to execute test code on a timed basis to detect soft errors. In reviewing the rejection of claims 11 and 22 (on page 3 of the Office action), Applicants respectfully note that the time-based feature of claims 11 and 22 is not considered. That is, there is no assertion that this feature is taught or suggested by Jiang et al. The Office action asserts that it would be obvious to follow the flow charts of Figs. 5 and 6 of the prior art patent to test and check errors of random access memory. Neither Fig. 5 nor Fig. 6 describes time-based error checking. Therefore, the prior art patent does not establish a *prima facie* case of obviousness under Section 103(a).

In the Office action, Quach was cited for teaching a number of features. However, it was not asserted that Quach would render it obvious to modify Jiang et al. to include performing time-based volatile memory checking routines (claim 11) or to include an automated memory checker configured to execute test code on a timed basis to detect soft errors (claim 22). As previously described, Quach teaches error checking while a processor is in its redundant execution mode. When a soft error is detected, the processor enters its split execution mode that enables uncorrupted data to be stored, identified, and used in order to return the processor to the program thread that was executing when the soft error was detected. Like the primary reference to Jiang et al., Quach does not teach or suggest time based error checking during periods in which the device is inactive.

Reconsideration of the patentability of claims 1, 11 and 22 and their dependent claims is respectfully requested.

B. Patentability of Independent Claim 17

Claim 17 describes an integrated circuit that includes a self-tester having stored test code, with the self-tester being responsive to a time-based test initialization signal for triggering periodic testing. The Office action rejects claim 17 over Jiang et al. in view of Quach. However, in the comparison of the claim language to the teachings of the prior art, no reference is made to responsiveness to a time-based test initialization signal. Similarly, the Office action does not cite either prior art reference for teaching "periodic testing." It is respectfully asserted that even if one were to modify the teachings of Jiang et al. as proposed in the Office action, the resulting circuit would not render Applicants' claimed invention obvious under Section 103(a). That is, the required *prima facie* case of obviousness has not been established by the Office action or by a careful reading of the two cited references. Reconsideration of claim 17 and its dependent claims is requested.

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited. In the case that any issues regarding this application can be resolved expeditiously via a telephone conversation, Applicants invite the Examiner to call Terry McHugh at (650) 969-8458.

Respectfully submitted,

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